

**FCH20N60 / FCA20N60 / FCA20N60\_F109**

**600V N-Channel MOSFET**

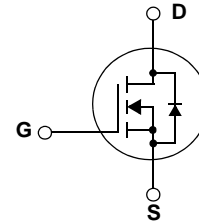
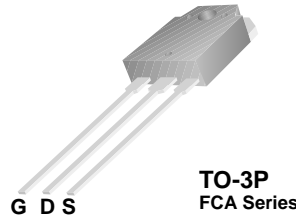
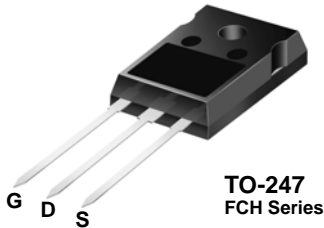
**Features**

- 650V @T<sub>J</sub> = 150°C
- Typ. R<sub>ds(on)</sub>=0.15Ω
- Ultra low gate charge (typ. Q<sub>g</sub>=55nC)
- Low effective output capacitance (typ. C<sub>oss,eff</sub>=110pF)
- 100% avalanche tested

**Description**

SuperFET™ is, Fairchild's proprietary, new generation of high voltage MOSFET family that is utilizing an advanced charge balance mechanism for outstanding low on-resistance and lower gate charge performance.

This advanced technology has been tailored to minimize conduction loss, provide superior switching performance, and withstand extreme dv/dt rate and higher avalanche energy. Consequently, SuperFET is very suitable for various AC/DC power conversion in switching mode operation for system miniaturization and higher efficiency.



**Absolute Maximum Ratings**

Symbol	Parameter	FCH20N60	FCA20N60	Unit
V <sub>DSS</sub>	Drain-Source Voltage	600		V
I <sub>D</sub>	Drain Current - Continuous (T <sub>C</sub> = 25°C) - Continuous (T <sub>C</sub> = 100°C)	20 12.5		A A
I <sub>DM</sub>	Drain Current - Pulsed (Note 1)	60		A
V <sub>GSS</sub>	Gate-Source voltage	± 30		V
E <sub>AS</sub>	Single Pulsed Avalanche Energy (Note 2)	690		mJ
I <sub>AR</sub>	Avalanche Current (Note 1)	20		A
E <sub>AR</sub>	Repetitive Avalanche Energy (Note 1)	20.8		mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5		V/ns
P <sub>D</sub>	Power Dissipation (T <sub>C</sub> = 25°C) - Derate above 25°C	208 1.67		W W/°C
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature Range	-55 to +150		°C
T <sub>L</sub>	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300		°C

**Thermal Characteristics**

Symbol	Parameter	Typ.	Max.	Unit
R <sub>θJC</sub>	Thermal Resistance, Junction-to-Case	--	0.6	°C/W
R <sub>θCS</sub>	Thermal Resistance, Case-to-Sink	0.24	--	
R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient	--	41.7	°C/W

## Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FCH20N60	FCH20N60	TO-247	-	-	30
FCA20N60	FCA20N60	TO-3P	-	-	30
FCA20N60	FCA20N60_F109	TO-3PN	-	-	30

## Electrical Characteristics T<sub>C</sub> = 25°C unless otherwise noted

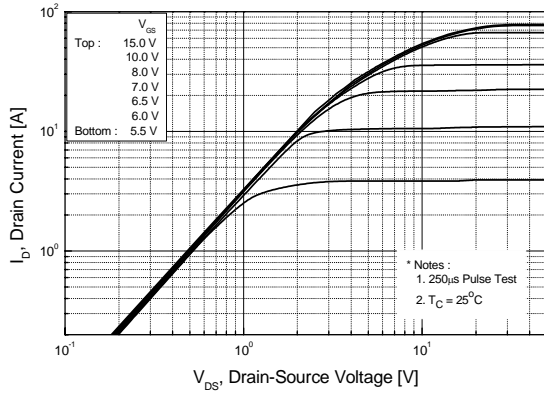
Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>Off Characteristics</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA, T <sub>J</sub> = 25°C	600	--	--	V
		V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA, T <sub>J</sub> = 150°C	--	650	--	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250μA, Referenced to 25°C	--	0.6	--	V/°C
BV <sub>DS</sub>	Drain-Source Avalanche Breakdown Voltage	V <sub>GS</sub> = 0V, I <sub>D</sub> = 20A	--	700	--	V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 600V, V <sub>GS</sub> = 0V	--	--	1	μA
		V <sub>DS</sub> = 480V, T <sub>C</sub> = 125°C	--	--	10	μA
I <sub>GSSF</sub>	Gate-Body Leakage Current, Forward	V <sub>GS</sub> = 30V, V <sub>DS</sub> = 0V	--	--	100	nA
I <sub>GSSR</sub>	Gate-Body Leakage Current, Reverse	V <sub>GS</sub> = -30V, V <sub>DS</sub> = 0V	--	--	-100	nA
<b>On Characteristics</b>						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	3.0	--	5.0	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = 10V, I <sub>D</sub> = 10A	--	0.15	0.19	Ω
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 40V, I <sub>D</sub> = 10A (Note 4)	--	17	--	S
<b>Dynamic Characteristics</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25V, V <sub>GS</sub> = 0V, f = 1.0MHz	--	2370	3080	pF
C <sub>oss</sub>	Output Capacitance		--	1280	1665	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		--	95	--	pF
C <sub>oss</sub>	Output Capacitance	V <sub>DS</sub> = 480V, V <sub>GS</sub> = 0V, f = 1.0MHz	--	65	85	pF
C <sub>oss eff.</sub>	Effective Output Capacitance	V <sub>DS</sub> = 0V to 400V, V <sub>GS</sub> = 0V	--	165	--	pF
<b>Switching Characteristics</b>						
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 300V, I <sub>D</sub> = 20A R <sub>G</sub> = 25Ω	--	62	135	ns
t <sub>r</sub>	Turn-On Rise Time		--	140	290	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		--	230	470	ns
t <sub>f</sub>	Turn-Off Fall Time		(Note 4, 5)	--	65	140
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> = 480V, I <sub>D</sub> = 20A V <sub>GS</sub> = 10V	--	75	98	nC
Q <sub>gs</sub>	Gate-Source Charge		--	13.5	18	nC
Q <sub>gd</sub>	Gate-Drain Charge		(Note 4, 5)	--	36	--
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current		--	--	20	A
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode Forward Current		--	--	60	A
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0V, I <sub>S</sub> = 20A	--	--	1.4	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0V, I <sub>S</sub> = 20A di <sub>F</sub> /dt = 100A/μs (Note 4)	--	530	--	ns
Q <sub>rr</sub>	Reverse Recovery Charge		--	10.5	--	μC

### NOTES:

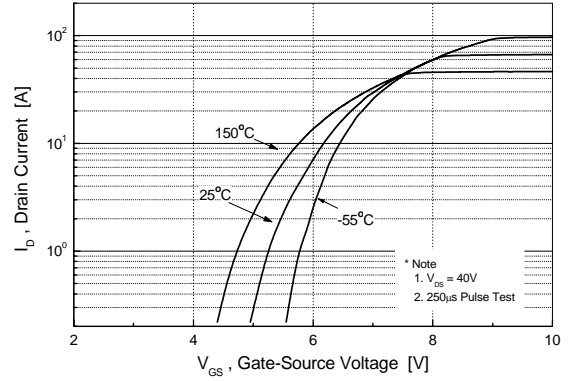
1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. I<sub>AS</sub> = 10A, V<sub>DD</sub> = 50V, R<sub>G</sub> = 25Ω, Starting T<sub>J</sub> = 25°C
3. I<sub>SD</sub> ≤ 20A, di/dt ≤ 200A/μs, V<sub>DD</sub> ≤ BV<sub>DSS</sub>, Starting T<sub>J</sub> = 25°C
4. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
5. Essentially Independent of Operating Temperature Typical Characteristics

## Typical Performance Characteristics

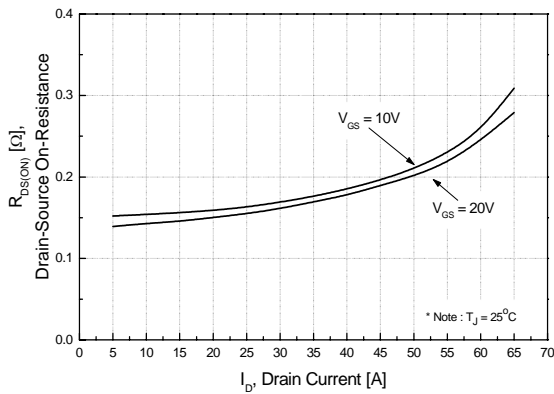
**Figure 1. On-Region Characteristics**



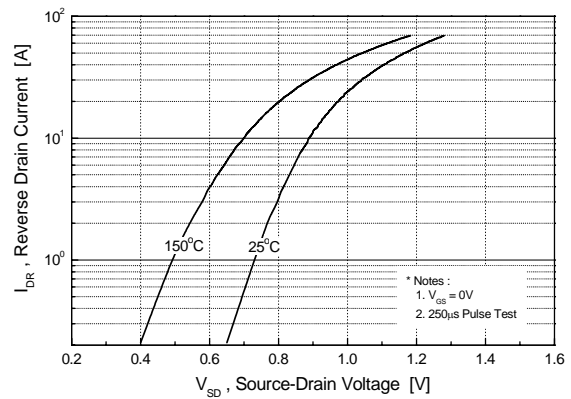
**Figure 2. Transfer Characteristics**



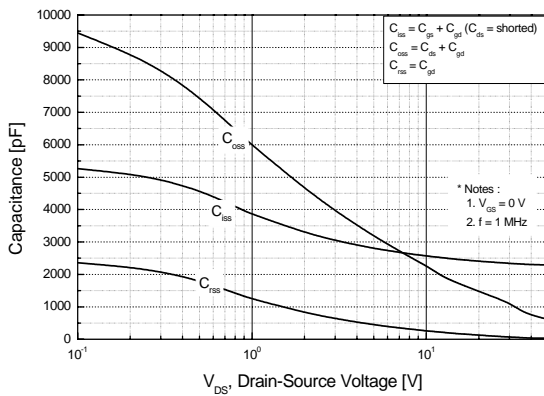
**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**



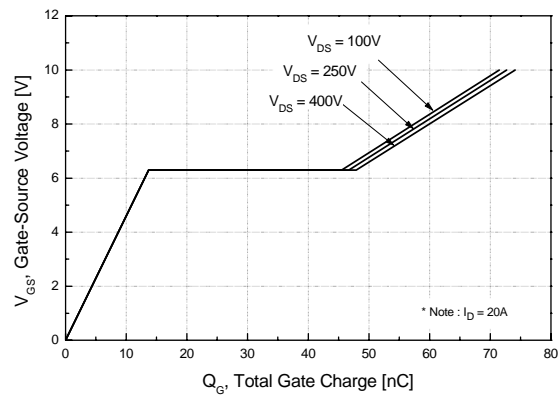
**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**



**Figure 5. Capacitance Characteristics**

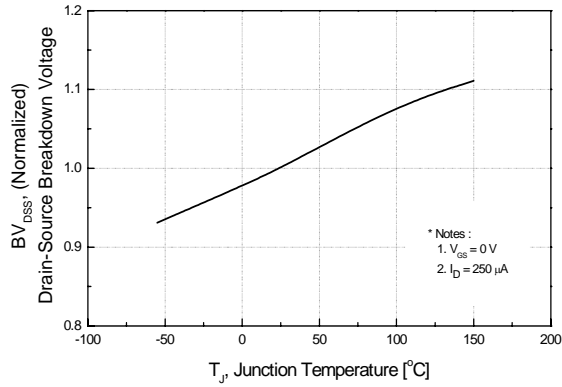


**Figure 6. Gate Charge Characteristics**

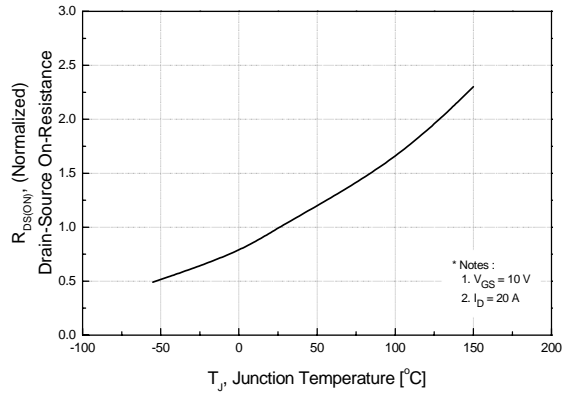


**Typical Performance Characteristics (Continued)**

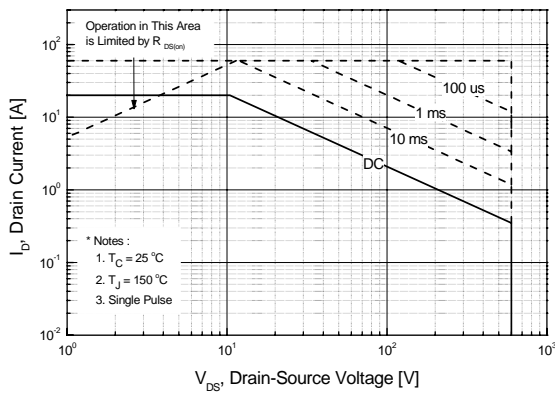
**Figure 7. Breakdown Voltage Variation vs. Temperature**



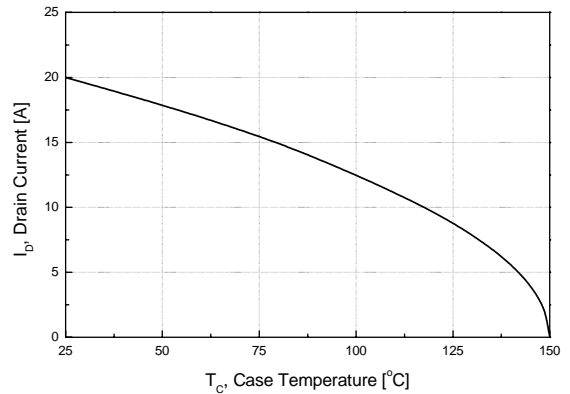
**Figure 8. On-Resistance Variation vs. Temperature**



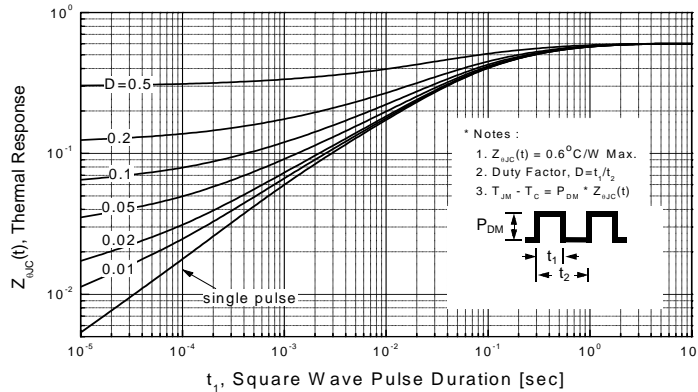
**Figure 9. Maximum Safe Operating Area**



**Figure 10. Maximum Drain Current vs. Case Temperature**



**Figure 11. Transient Thermal Response Curve**



**Gate Charge Test Circuit & Waveform**



**Resistive Switching Test Circuit & Waveforms**



**Unclamped Inductive Switching Test Circuit & Waveforms**

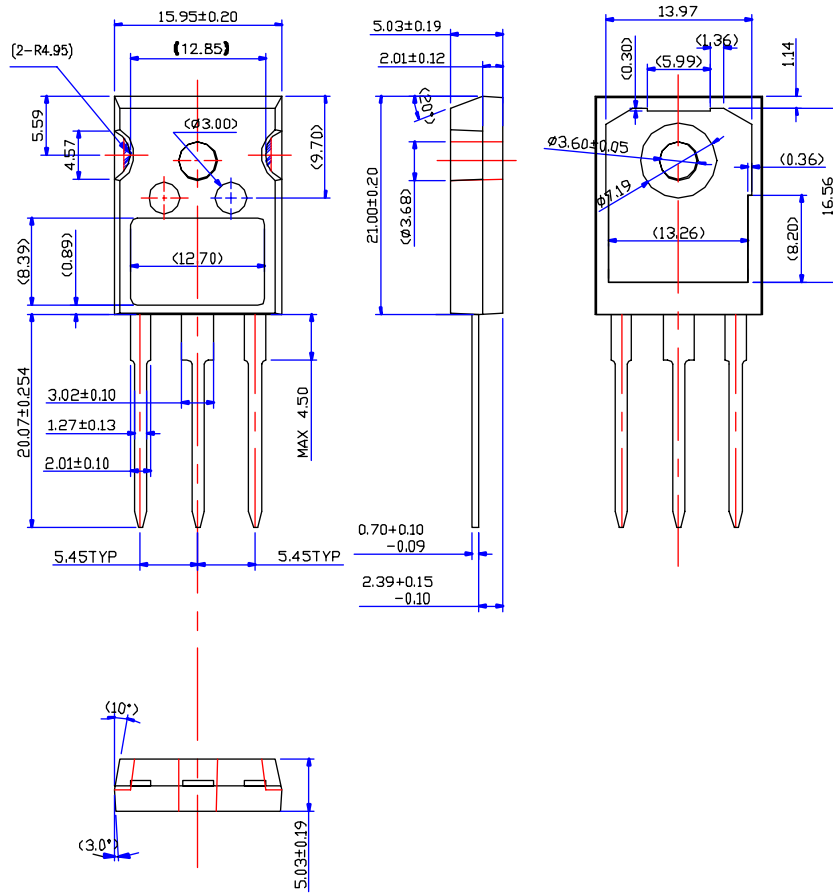


**Peak Diode Recovery dv/dt Test Circuit & Waveforms**



**Mechanical Dimensions**

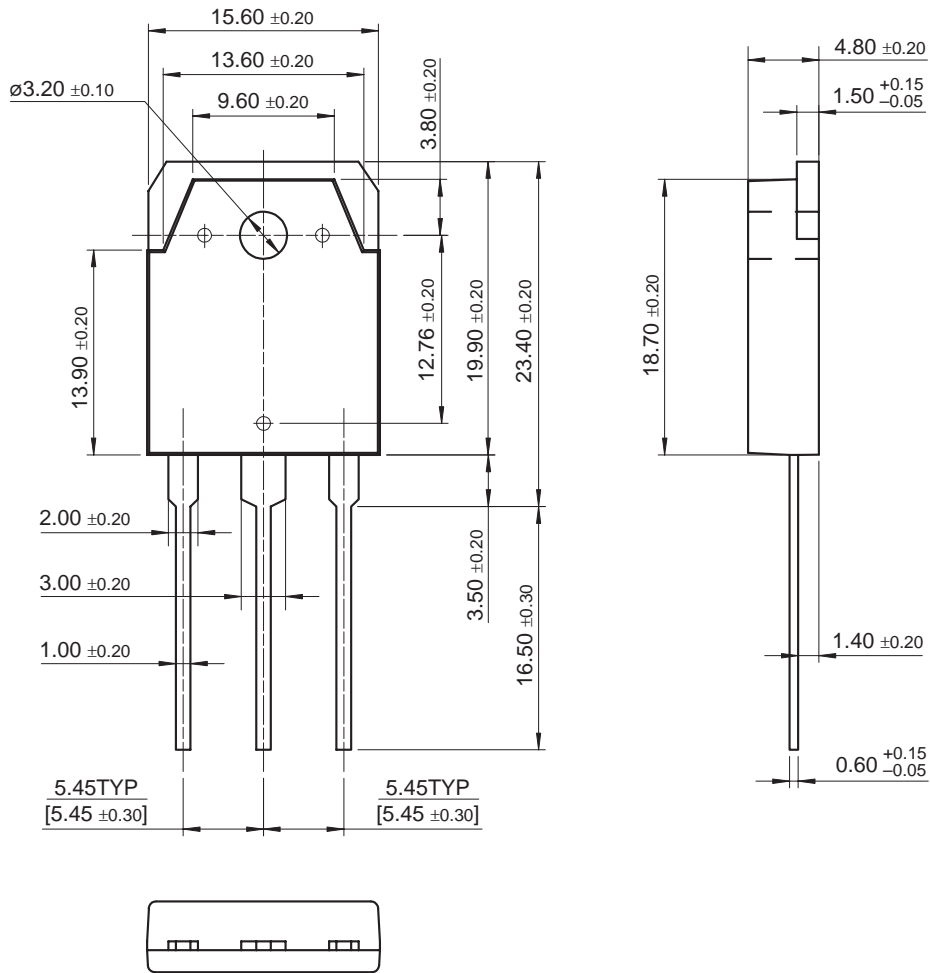
**TO-247AD (FKS PKG CODE 001)**



Dimensions in Millimeters

Mechanical Dimensions (Continued)

TO-3P

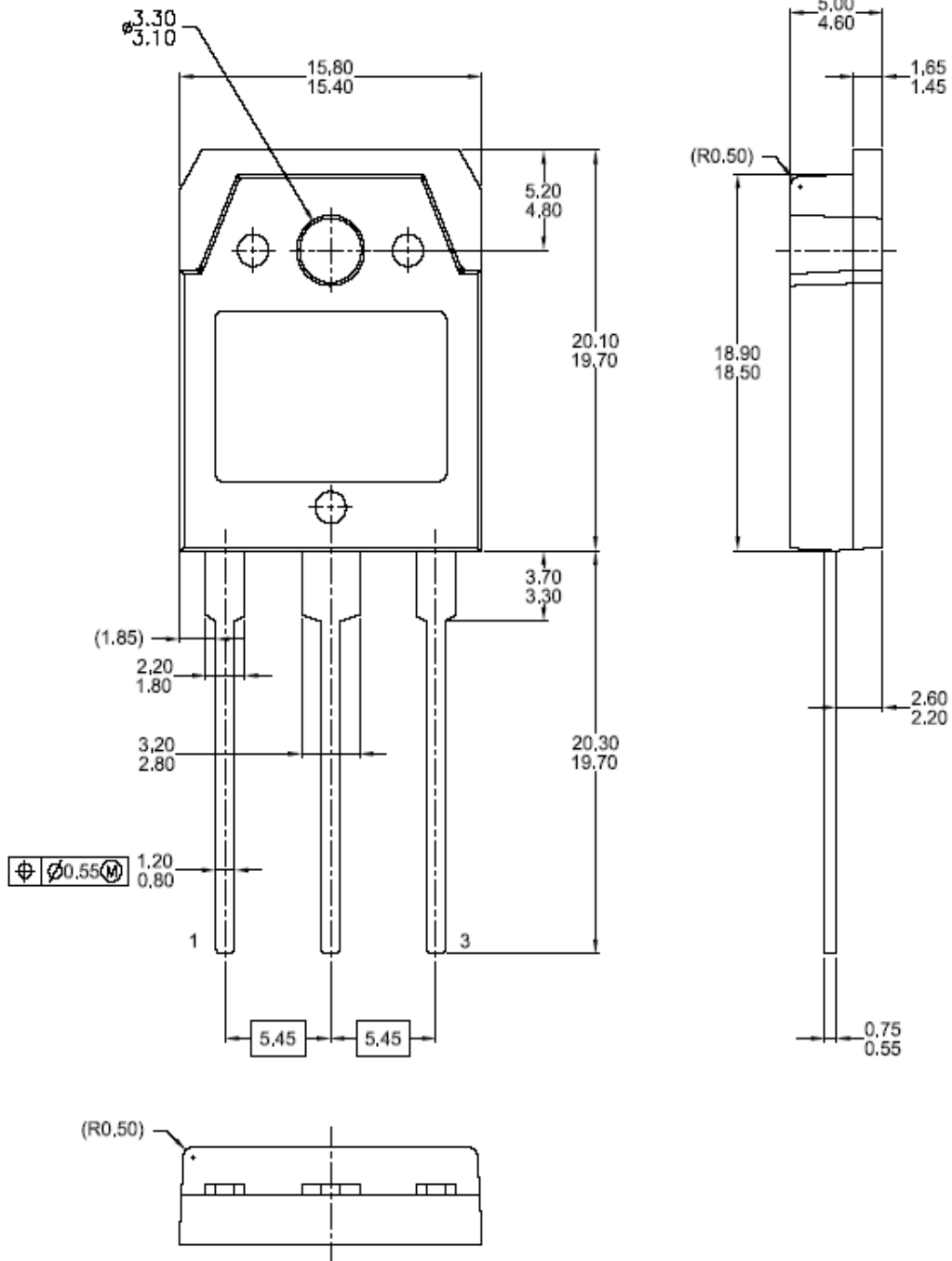


Dimensions in Millimeters



**Mechanical Dimensions** (Continued)

**TO-3PN**




Dimensions in Millimeters



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